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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,256	02/19/2004	Hsin-Shih Wang	FTCP0031USA	2255

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,256	WANG, HSIN-SHIH	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/708,256 filed on 2/19/2004. Claims 1-22 remain pending in the application.

Claim Objections

2. Claims 1 and 15 are objected to because of the following informalities: "identical device characteristic" needed clearly defined to be more specific. Claim 15, lines 2-3, "a plurality of basic unit" should be changed to –a plurality of basic units--. Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1 and 15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,902,957 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claim and the claims in the instant application refer to a method for forming an IC comprising a semiconductor body

comprising a plurality of basic units, each unit including at least of a logic module, at least one driver module and at least a storage module and is positioned on the semiconductor body; and a metal layer upon the body is used to program the modules to be as a logic function and storage element. It well known to practitioners in the art to recognize that each basic unit has identical device and the logic function and storage element correspond to non-clocked logic circuit and clocked logic circuit. Since the basic units can be used to form non-clocked logic circuit and clocked logic circuit, they can be placed anywhere on the semiconductor body.

5. Claims 1 and 15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,902,957 B2 in view of Friend et al. (US 2003/0140080 A1). Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claim and the claims in the instant application refer to a method for forming an IC comprising a semiconductor body comprising a plurality of basic units, each unit including at least of a logic module, at least one driver module and at least a storage module and is positioned on the semiconductor body; and a metal layer upon the body is used to program the modules to be as a logic function and storage element. The claim patent does not teach using a series of cascaded transistors to form non-clocked logic circuit or clocked logic circuit. Friend et al. teach using a series of cascaded transistors to form non-clocked logic circuit or clocked logic circuit (Fig. 3A-3B, 5; at least see [0062-0063]). Utilizing the series of cascaded transistors as taught by Friend in the patent claim would have been obvious to practitioners in the art at the

time the invention was because the non-clocked logic circuit and clocked logic circuit can be formed as expected by programming cascaded transistors (forming appropriate interconnection) using a metal layer on the semiconductor body.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (6,902,957 B2).

8. As to claim 1 and 15, Wang et al. teach a method for forming (fabricating) an IC having a semiconductor body comprising forming a plurality of basic units on the semiconductor body, each of the basic units having an identical device characteristic (Fig. 3, basic unit 42); and forming at least a layout layer (metal programmable integrated circuit) to program the basic units for generating a clocked logic circuit (synchronous logic circuit or storage module) and a non-clocked logic circuit (logic operation module) without placing restrictions on positions of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body (see at least summary; col.

6 lines 32-67; col. 7 lines 1-8; col. 7 lines 54-67; col. 8 lines 1-25; col. 10 lines 60-67; col. 11 lines 1-10).

9. As to claims 2-3, 16, 11 and 21, Wang et al. teach forming basic units any where on the semiconductor body including transistors that are MOS transistors (art inherent) (col. 10 lines 40-67).

10. As to claims 4-5, Wang et al. utilizing the layout layer (metal layer programmable) to program a basic unit/basic units for generating the clocked logic circuits (col. 10 lines 40-67; col. 11 lines 1-32).

11. As to claims 6-7 and 13-14, Wang et al. utilizing the layout layer (metal layer programmable) to program a basic unit/basic units for generating the non-clocked logic circuits (col. 8 line 26 to col. 10 line 59).

12. As to claims 8, 12, 17-18 and 21-22, Wang et al. teach forming basic units any where on the semiconductor body including transistors that are NMOS and PMOS transistors (art inherent) (col. 10 lines 40-67).

13. As to claims 9 and 19, remarks set forth in rejection of claims 1 and 15 equally apply. In addition, Wang et al. utilizing metal layers to establish partial traces routed among the transistors to form non-clocked logic circuit or clocked logic circuit on the semiconductor body (col. 10 lines 10-67). These teachings clearly suggest that each basic unit having a plurality of first transistors cascaded in a series and a plurality of second transistors cascaded in a series in order to form the non-clocked logic circuit or clocked logic circuit.

14. As to claims 10 and 20, Wang et al. teach metal layers under the metal layer establish partial traces routed among the transistors. That is, the actual function of the driver module or storage module is enable after a photomask pattern is used by a following semiconductor process for programming traces related to each node (col. 10 lines 40-67; col. 11 lines 1-10). This clearly suggests that the first transistors are not electrically connected to the second transistors before the traces are programmed because the actual function of the non-clocked logic circuit (driver module) or clocked logic circuit (storage module or flip flop or latch) is enable after photomask pattern is used by a following semiconductor process for programming traces related to each node (col. 10 lines 40-67; col. 11 lines 1-10).

15. Claim 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Friend et al. (US 2003/0140080 A1).

16. As to claims 1 and 15, Friend et al. teach an IC and a method of forming (fabricating) an IC having a semiconductor body comprising forming a plurality of basic units (domino logic gate) on the body, each having an identical device characteristic (Fig. 3). A domino logic gate can be converted into a latch that also performs logic. In Fig. 3B, clocked transistors 211 and 229 could be conditionally clocked (using different signals on the transistor gates known as qualified clocks). When the latch if not being loaded, the two transistors 211 and 229 are both off, causing the output node 215 to float, thereby holding the logic value (0062-0063). Thus, Friend et al. teach that the domino logic gate corresponding to basic unit can be used to program as logic circuit function (non-clocked logic circuit) or flip flop or latch (clocked logic circuit). These

domino logic gates comprise transistors (first series of cascaded transistors and second series of cascaded transistors as shown on Figs. 3 or 5). Metal layer(s) are known and used to form interconnection or traces between transistors to form logic circuit function or flip flop or latch. Since the domino logic gates can be used to form logic circuit function and flip flop or latch, they can be placed anywhere on the semiconductor body without placement restrictions in order to provide a wide variety of possible implementation (0062, 0063, 0079).

17. As to claims 9 and 19, remarks set forth in rejecting claims 1 and 15 equally apply. Figs. 3A-3B show first transistors cascaded in a series and second transistors cascaded in a series within the domino logic gate in order to form a clocked logic circuit (flip flop or latch) and non-clocked logic circuit (logic circuit function).

18. As to claims 2-3, 16, 11 and 21, Friend et al. teach forming basic units (domino logic gates) including transistors that are CMOS transistors (0063).

19. As to claims 4-5, Friend et al. teach utilizing the layout layer (metal layer is art inherent) to program a basic unit/basic units for generating the clocked logic circuits (0062-0063).

20. As to claims 6-7 and 13-14, Friend et al. teach utilizing the layout layer (metal layer is art inherent) to program a basic unit/basic units for generating the non-clocked logic circuits (0062-0063).

21. As to claims 8, 12, 17-18 and 21-22, Friend et al. teach forming CMOS transistors (PMOS and NMOS) within domino logic gates (basic units) (Fig. 3, 5, 0063).

22. As to claims 10 and 20, Friend et al. teach utilizing domino logic gates having first transistors cascaded in a series and second transistors cascaded in a series to form logic circuit function (non-clocked logic circuit) or flip flop or latch (clocked logic circuit). These teachings suggest that the first transistors are not electrically connected to the second transistors before the traces are programmed because by not connecting between the first and second transistors before the traces are programmed the domino logic gates (basic units) can used (programmed or formed) as non-clocked logic circuit (logic circuit function) or clocked logic circuit (flip flop or latch).

23. Claim 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Gheewala et al. (6,445,065 B1).

24. As to claims 1 and 15, Gheewala et al. teach a method for forming a user customizable IC having separate regions for different types of core cells (basic units) to form synchronous and asynchronous core cells (Fig. 3 shows semiconductor body having basic units; Fig. 5 shows synchronous core cell and Fig. 6 shows asynchronous core cell. The asynchronous core cell is non-clocked logic circuit and synchronous core cell is clocked logic circuit. Gheewala et al. teach that current design approaches provided that high-drive cells are placed throughout the IC without any restrictions, even in places where the power bussing is not adequate (col. 20-24). Gheewala et al. also teach as is well known in the art, asynchronous cells may connected in various ways to provide a synchronous function including the use of a clock (clocked logic circuit). These clearly suggest that it is well known that having basic units from which asynchronous cells (non-clocked logic circuit) and/or synchronous cells (clocked logic

circuit) can be formed. The formation of asynchronous cells and synchronous cells is obtained by interconnection using a metal layer (col. 8 lines 4-60).

25. As to claims 9 and 19, remarks set forth in rejection of claims 1 and 15 equally apply. Fig. 6B shows first transistors cascaded in a series and second transistors cascaded in a series.

26. As to claims 2-3, 16, 11 and 21, Gheewala et al. teach forming basic units including transistors that are CMOS transistors (Fig. 6B).

27. As to claims 4-5, Gheewala et al. teach utilizing the layout layer (metal layer) to program a basic unit/basic units for generating the clocked logic circuits (Fig. 5).

28. As to claims 6-7 and 13-14, Gheewala et al teach utilizing the layout layer (metal layer) to program a basic unit/basic units for generating the non-clocked logic circuits (Fig. 6).

29. As to claims 8, 12, 17-18 and 21-22, Gheewala et al. teach forming CMOS transistors (PMOS and NMOS) within each basic unit (Figs. 5-6, col. 9 lines 52-67; col. 10 lines 1-21).

30. As to claims 10 and 20, Gheewala et al teach utilizing first transistors cascaded in a series and second transistors cascaded in a series to form asynchronous cell (non-clocked logic circuit) (Fig. 6). These teachings suggest that the first transistors are not electrically connected to the second transistors before the traces are programmed because by not connecting between the first and second transistors before the traces are programmed because in this way different logic functions may also be implemented

using combinations of synchronous core cell and asynchronous core cell (col. 9 lines 52-67; col. 10 lines 1-21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek